REMARKS

Claims 1-17 are pending in the application. Claims 1-12 and 14 have been withdrawn from consideration and claims 13 and 15-17 stand rejected.

Claim Rejections under 35 U.S.C. §112, Second Paragraph

Claims 15 to 17 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Taking the Examiner's comments into consideration claims 15-17 have been amended. Therefore, withdrawal of the rejection of the rejection of Claims 15 to 17 under 35 U.S.C. §112, second paragraph, is respectfully requested.

Claim Rejections under 35 U.S.C. §102(b)

Claims 13 and 15 to 17 have been rejected under 35 U.S.C. §102(b) as being anticipated by Takeuchi Yakiharu (Japanese Patent 2000-323645).

At the outset it should be noted that the grounds of rejection have changed from that supplied in the Office Action mailed December 16, 2005. In that previous Office Action the prior art relied upon was Gorczyca (U.S. 5,492,586) and Eichelberger (U.S. 5,111,278). In this rejection the Examiner relies on Takeuchi Yakiharu (Japanese Patent 2000-323645) as prior art. .

The present invention is an electronic parts packaging structure in which five embodiments are described in the specification. Claims 13 and 15-17 which are currently being prosecuted are directed to the first embodiment as illustrated in Figures 2A-2H. The first embodiment includes, as shown in Figure 2A, a base substrate (24) on which a wiring substrate is prepared. Through-holes (24a) are provided in the base substrate (24) and through-hole plating layers (24b) are connected to a first wiring patterns (28). A first interlayer insulation film (30) is placed on top of the first wiring patterns (28). First via holes (30x) are formed on the first interlayer insulation film (30). A second wiring patterns (28a) is formed on the first interlayer insulation film (30). As shown in Figure 2B, a first resin film (32a) is formed on the second wiring patterns (28a) and the first interlayer insulation film (30). As shown in Figure 2C, a semiconductor chip (20) (electronic parts)is embedded in the first resin film (32a). Connection pads (21a) (connection terminals) are exposed on the element formation surface of the semiconductor chip (20). As shown in Figure 2D, a second interlayer insulation film (32) is created composed of the first resin film 32a (first insulating film) and a second resin film (32b) (second insulation film). As shown in Figure 2E, via holes (32x) are formed in the second interlayer insulation film (32) on the connection pads (21a) of the semiconductor chip (20) and on the second wiring patterns (28a). As shown in Figure 2G, a third wiring patterns (28b) (upper wiring patterns) are connected to the connection pads (21a) of the semiconductor chip (20) and to the second wiring patterns (28a) through the second via holes (32x), formed on the second interlayer insulation film (32). Finally, an upper semiconductor chip (20x) (upper electronic parts) with bumps (23) which are flip-chip bonded to the connection portions (28z) of the third wiring patterns (28b).

Takeuchi Yakiharu (Japanese Patent 2000-323645) describes a semiconductor device. The Examiner relies on Figure 4 of Takeuchi Yakiharu (Japanese Patent 2000-323645) a copy of which we have enlarged and labeled according to the Examiner's assertions. The Examiner asserts that Takeuchi Yakiharu (Japanese Patent 2000-323645) describes a substrate (20), a first insulation film (26b), a second insulation film (26c), a wiring pattern (22d), electronic parts (12), upper electronic parts (12 again) and bumps (38).

The Examiner asserts that all elements of claim 13 are disclosed in Takeuchi.

In Fig. 4 of Takeuchi, a semiconductor chip 12 is buried in the three insulating films 26a - 26c, respectively. Since the Examiner points out that via holes are formed in the insulating film on the semiconductor 12 like claim 13 in this application, the lowermost semiconductor chip 12 in Fig. 4 must correspond to the electronic parts of claim 13 (via holes do not exist in the insulating film 26b, 26c on the second and third semiconductor chip 12 from the bottom to order).

In Fig 4 of Takeuchi, the lowest semiconductor chip 12 contacts with the wiring pattern 22a of the wiring substrate (resin substrate) 20. In Claim 13, as shown in Fig. 2H, the electronic parts 20x is buried in the first insulating film 32a in the state that a lower portion of the first insulating film 32a exists between the electronic parts 20x and the wiring substrate 24 (the electronic parts 20x is buried in intermediate position of the thickness of the first insulating film 32a).

The first insulating film functions as adhesive layer for gluing the electronic parts to the wiring substrate by remaining the lower portion of the fist insulating film.

According, claim 13 has been amended such that the lower portion of the first insulating film exists between the electronic parts and the wiring substrate.

In addition, since the lowermost semiconductor chip 12 in Fig. 4 of Takeuchi corresponds to the electronic parts of claim 13, the second insulating film of claim 13 corresponds to the insulating film 26b which covers the electronic parts. In claim 13, since the via holes are formed by laser after the first and second insulating film are formed, the via holes formed in the first and second insulating films on the wiring pattern is formed as straight shape. In Fig. 4 of Takeuchi, however, since the interlayer connection (corresponding to the via hole on the wiring pattern in claim 13) is constructed by stacking two wiring patterns, the interlayer connection is formed as step shape.

Accordingly, claim 13 has further been amended such that the via holes on the wiring pattern have an identical inner surface.

Also, in Fig. 4 of Takeuchi, the bump 38 of the uppermost semiconductor chip 12 is flip-chip bonded to the wiring pattern 22d formed on the upper side insulating film 26c and not the insulating film 26b covering the lowermost semiconductor chip 12. Accordingly, claim 13 has been amended such that the second insulating film contacts with the electronic parts as a single layer.

Therefore, claim 13 patentably distinguishes over the prior art of record by reciting,

> "An electronic parts packaging structure comprising: a wiring substrate including a wiring pattern; a first insulation film formed on the wiring substrate; an electronic parts having a connection terminal on an element formation surface, the electronic parts being buried in the first insulation film in a state where the connection terminal is directed upward and being mounted in a state where a backside of the electronic parts is not in contact with the wiring substrate, and a lower portion of the first insulating film exists between the electronic parts and the wiring substrate; a second insulation film for covering the electronic parts, and whose

> upper surface is flat over a whole on the wiring substrate, and the second insulation film contacting with the electronic parts as a single layer, and; first via holes formed in a predetermined portion of the first and second insulation films on the wiring pattern, and having an identical inner surface; second via holes formed in a portion of the second insulating film on the connection terminal of the electron parts; via holes respectively formed in a predetermined portion of the first and second insulation films on the wiring pattern and the connection terminal; an upper wiring pattern formed as a single wiring on the second insulation film, the upper wiring pattern being connected to the wiring pattern and the connection terminal through the via holes; and an upper electronic part with bumps which are flip-chip bonded to connection portions of the upper wiring pattern, the connection pad which directly contacts the upper surface of the second insulating film." (Emphasis Added)

Therefore, withdrawal of the rejection of claims 13 and 15 to 17 under 35 U.S.C. §102(b) as being anticipated by Takeuchi Yakiharu (Japanese Patent 2000-323645) is respectfully requested.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 13 and 15-17, as amended, are believed to be patentable and in condition for allowance, which action, at an early date, is respectfully requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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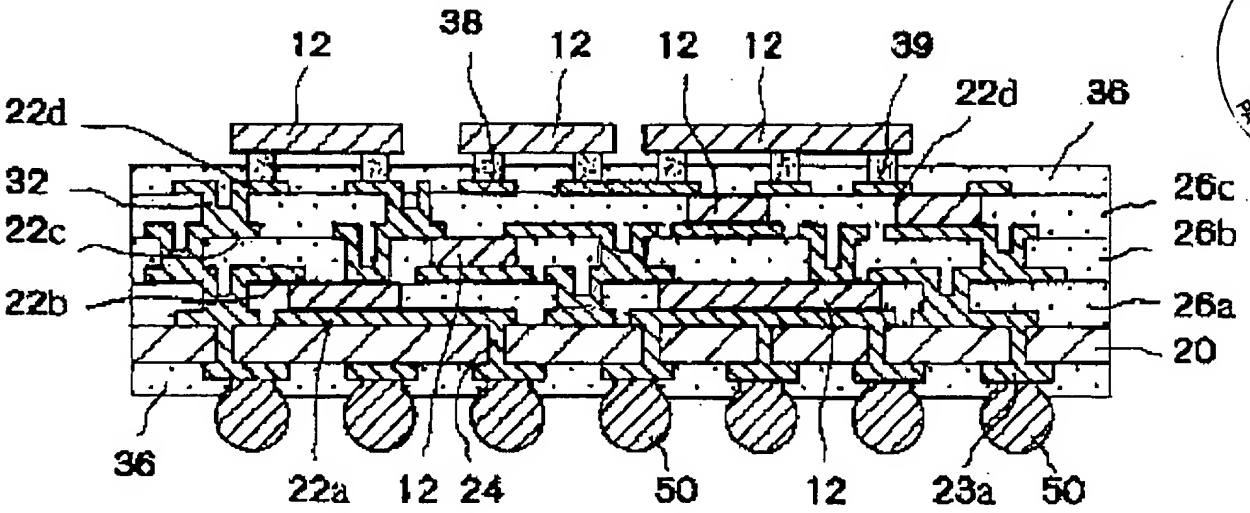
FIG.4 (2000-323645)



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